Karri Chandra Sekhar

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Education

Indian Institute of Technology Bhubaneswar CGPA: 7.81 (Till 5th Sem)
B.Tech in Electronics and Communication Engineering *2023 – Present*

Sasi Educational Institute, Velivennu Score: 467/500
CBSE (Class 11 & 12) *2021 – 2023*

Technical Skills

Languages: Verilog, SystemVerilog (Learning), C/C++, CUDA
Protocols & IPs: AMBA, UART, GRLIB, NOEL-V (Cobham Gaisler)
Tools: Xilinx Vivado, Vitis, Matlab, LTSpice, Cadence, KiCad, Altium
Boards: Basys3, ZedBoard (Zynq-7000), PYNQ-Z2, ZCU104 (Zynq UltraScale+)
Currently Learning: SystemVerilog, UVM, Physical Design (RTL-to-GDSII)

Internships & Achievements

Intern – GPU Programming and Benchmarking May 2025 – Jul 2025
Under Dr. Devashree Tripathy, CSE, IIT Bhubaneswar

- Acquired foundational knowledge in **CUDA** development, **GPU microarchitecture**, and parallel computing.
- Implemented optimized **matrix multiplication kernels** using advanced memory management techniques.
- Developed custom benchmarking scripts for GPU-based **convolution** and **Deriche filtering**; reviewed **NVIDIA H100** architecture.

Awards

- Awarded **INR 1,00,000 LPU Scholarship**; Secured **53rd rank** in LPU NEST exam.
- Secured **Top 30** in Sense2Scale Hackathon 2025 (Respire India: Low-Cost Respiratory Monitoring System).

Projects

Linux Boot on PYNQ-Z2 (Zynq SoC) | *Vivado, SD Image* Jan 2026

- Configured **Zynq PS** using Vivado block design and successfully **booted Linux** on the **PYNQ-Z2** board via SD card.
- Explored **PS-PL integration** and tested basic peripheral communication (GPIO, UART) from Linux userspace.

AMBA AHB Slave Integration with NOEL-V on ZCU104 | *Verilog, GRLIB, Vivado* Dec 2025

- Studied **AMBA AHB** protocol and explored **GRLIB** open-source IP library with **NOEL-V** RISC-V SoC framework.
- Integrated a **custom AHB slave** peripheral into the NOEL-V subsystem targeting **ZCU104** (Zynq UltraScale+).
- Gained hands-on understanding of **SoC bus interconnect** design and IP integration workflows.

RISC-V Processor Design (Single-Cycle, Multi-Cycle & Pipelined) | *Verilog, Vivado* Dec 2025

- Designed a **32-bit RISC-V (RV32I)** processor, progressively building **single-cycle, multi-cycle, and 5-stage pipelined** architectures.
- Implemented **hazard detection and data forwarding** logic; supported R/I/S/B-type instructions.
- Synthesized and validated on FPGA using Xilinx Vivado with functional verification through testbenches.

UART Protocol Implementation on FPGA | *Verilog, Vivado, PuTTY* May 2025

- Designed **UART** transmitter and receiver modules with **configurable baud rate** and **FIFO buffers**.
- Verified reliable data transmission through hardware testing using PuTTY terminal.

BFLOAT16 Arithmetic Implementation on FPGA | *Verilog, Vivado, Basys3* Apr 2025

- Designed **bfloat16** floating-point addition, subtraction, and multiplication units in Verilog.
- Synthesized and tested on **Basys3 FPGA**, enabling results via switch inputs and LED outputs.

Type-2 PLL Circuit Design + PCB | *KiCad, Oscilloscope* Dec 2024

- Designed a **Type-2 PLL** for stable frequency amplification; developed **PCB** in KiCad, soldered and tested with oscilloscope.

Position of Responsibilities & Extra-Curricular

NSS Coordinator, IIT Bhubaneswar (Aug 2024 – Present) – Organizing **blood donation camps**, **plantation drives**, and headed **special camps**; attended **Youth Leadership Training (YLT)** camp. Mentoring junior students in NSS activities, fostering teamwork and community engagement.
Core Head, Sponsorship & Marketing Team – **Wissenaire** (2023–24) and **Pravaah** (2025–Present), IIT Bhubaneswar.
Core Head, **Sah Astitva** (Animal Welfare Society), IIT Bhubaneswar (Sep 2024 – Present).